[MUX SCAN CELL] WITH DELAY CIRCUIT FOR REDUCING HOLD-TIME VIOLATIONS]

Abstract of Disclosure

A mux scan cell includes a multiplexer having a first input node for receiving raw data, a second input node for receiving test data, an output node, a selection node, and a delay circuit electrically connected between the second input node and the output node for prolonging a traveling time which the test data takes to travel from the second input node to the output node. The mux scan cell also includes a flip-flop connected to the multiplexer. With the delay circuit, the traveling time of the test data is prolonged such that the traveling time which the test data takes to travel from the second input node to the output node simulates a sum of a traveling time in which the raw data travels through a combinational logic and a traveling time in which the raw data travels from the first input node to the output node.

Figures